WHAT IS CLAIMED IS:

1. An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a multi-strobe generator for generating a multi-strobe having a plurality of strobes, of which phases are different by a small amount;

an output data transition point detector for detecting a timing of rising or falling of a waveform of said output data based on said multi-strobe;

a reference clock transition point detector for detecting a timing of rising or falling of a reference clock outputted by said semiconductor device accompanying said output data, wherein said reference clock is a signal to set a timing of passing said output data, based on said multi-strobe; and

a judging unit for judging quality of said semiconductor device based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector.

2. An apparatus for testing a semiconductor device as claimed in claim 1, wherein said judging unit judges quality of said semiconductor device based on whether or not a phase difference between said timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector is within a predetermined range.

3. An apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator generates a first multi-strobe in order to detect a transition point of a value of said output data and a second multi-strobe in order to detect a transition point of a value of said reference clock.

4. An apparatus for testing a semiconductor device as claimed in claim 3, further comprising a level comparator for changing said output data and said reference clock into digital data represented by H logic or L logic, wherein

said output data transition point detector detects a value of said output data changed into said digital data in regard to a phase of each of strobes of said first multi-strobe, and if a value of said output data in regard to a phase of a first strobe of said first multi-strobe and a value of said output data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

said reference clock transition point detector detects a value of said reference clock changed into said digital data in regard to a phase of each of strobes of said second multi-strobe, and if a value of said reference clock in regard to a phase of a third strobe of said second multi-strobe and a value of said reference clock in regard to a phase of a fourth strobe adjacent to said third strobe are different then determines said phase of said third strobe as said transition point of said value of said reference clock, and

said judging unit judges quality of said semiconductor device based on said transition point of said value of said output data and said transition point of said value of said reference

clock.

5. An apparatus for testing a semiconductor device as claimed in claim 4, wherein said judging unit judges quality of said semiconductor device based on whether or not a difference between a strobe number of said first multi-strobe indicating which timing of a strobe of said first multi-strobe said output data transition point detector detects said transition point of a value of said output data and a strobe number of said second multi-strobe indicating which timing of a strobe of said second multi-strobe said reference clock transition point detector detects said transition point of a value of said reference clock at is within a predetermined range.

6. An apparatus for testing a semiconductor device as claimed in claim 4, wherein said judging unit comprises a memory for storing a reference table to set quality of said semiconductor device about a combination of said strobe number of said first multi-strobe, in which said transition point of a value of said output data is detected and said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected, and judges quality of said semiconductor device based on said reference table.

7. An apparatus for testing a semiconductor device as claimed in claim 4, wherein said output data transition point detector comprises a means for detecting whether a value of digital data in regard to said transition point of a value of said output data changes from said H logic to said L logic or changes from said L logic to said H logic.

8. An apparatus for testing a semiconductor device as claimed in claim 4, wherein said output data transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data are detected.

9. An apparatus for testing a semiconductor device as claimed in claim 1, further comprising a glitch detector for detecting existence of a glitch in regard to said output data based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector.

10. An apparatus for testing a semiconductor device as claimed in claim 9, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

11. An apparatus for testing a semiconductor device as claimed in claim 9, wherein said glitch detector detects existence of a glitch in regard to said output data based on said transition point of a value of said output data.

12. An apparatus for testing a semiconductor device as claimed in claim 11, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data are more than or equal to two.

13. An apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator comprises a plurality of delay devices having different delay times, supplies

a strobe to each of said plurality of delay devices and outputs a plurality of strobes, delayed to have a different time delay respectively and outputted by said plurality of delay devices, as said multi-strobe.

14. An apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to each of said plurality of delay devices connected in cascade and generates said multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

15. An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generator for generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data;

a reference phase measuring unit for measuring an output timing, which is a signal to set a timing of passing said output data, being a timing of rising or falling of a waveform of a reference clock outputted by said semiconductor device accompanying said output data;

a reference phase memory for memorizing said output timing;

a transition point detector for detecting a transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring unit for measuring a phase difference between said output timing and said transition point of a value of said output data; and

a judging unit for judging quality of said semiconductor device based on said phase difference.

16. An apparatus for testing a semiconductor device as claimed in claim 15, wherein said first multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to said plurality of delay devices connected in cascade, and generates said first multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

17. An apparatus for testing a semiconductor device as claimed in claim 15, wherein said transition point detector comprises a means for changing said output data into digital data represented by H logic or L logic, and

said transition point detector detects a value of said output data in regard to a phase of each of strobes of said first multi-strobe, and if a value of digital data in regard to a phase of a first strobe of said first multi-strobe and a value of digital data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data.

18. An apparatus for testing a semiconductor device as claimed in claim 17, wherein said transition point detector comprises a means for detecting whether said value of digital data in regard to said transition point changes from said H logic to said L logic or changes from said L logic to said H logic.

19. An apparatus for testing a semiconductor device as claimed in claim 18, wherein said transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output

data if a plurality of said transition points of a value of said output data is detected.

20. An apparatus for testing a semiconductor device as claimed in claim 15, wherein said reference phase measuring unit comprises:

a means for generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said reference clock;

a means for detecting said transition point of a value of said reference clock based on said second multi-strobe; and

a means for calculating said output timing of said reference clock based on a strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

21. An apparatus for testing a semiconductor device as claimed in claim 20, wherein said reference phase memory stores said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

22. An apparatus for testing a semiconductor device as claimed in claim 21, wherein said first multi-strobe generator sets a phase of said first multi-strobe based on said strobe number of said second multi-strobe stored by said reference phase memory.

23. An apparatus for testing a semiconductor device as claimed in claim 15, further comprising a glitch detector for detecting existence of a glitch in regard to said transition point of a value of said output data.

24. An apparatus for testing a semiconductor device as claimed in claim 23, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

25. An apparatus for testing a semiconductor device as claimed in claim 23, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data detected by said transition point detector are more than or equal to two.

26. A method for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data;

an output data transition point detecting step of detecting a timing of rising or falling of a waveform of said output data based on said first multi-strobe;

a second multi-strobe generating step of generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to a reference clock, which is a signal to set a timing of passing said output data, said reference clock being outputted by said semiconductor device accompanying said output data;

a reference clock transition point detecting step of detecting a timing of rising or falling of a waveform of said reference clock based on said second multi-strobe; and

a judging step of judging quality of said semiconductor device based on said timing of rising or falling of a waveform of said output data detected in said output data transition point

detecting step and said timing of rising or falling of a waveform of said reference clock detected in said reference clock transition point detecting step.

27. A method for testing a semiconductor device as claim in claim 26, further comprising a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data, wherein

said judging step judges quality of said semiconductor device further based on existence of said glitch detected in said glitch detecting step.

28. A method for testing a semiconductor device based on output data of said semiconductor device, comprising:

a reference phase measurement step of measuring an output timing of a reference clock, which is a signal to set a timing of passing said output data, said reference clock being outputted by said semiconductor device accompanying said output data;

a reference phase memorizing step of memorizing said output timing;

a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data;

an output data transition point detecting step of detecting said transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring step of measuring a phase difference between said output timing and said transition point of a value of said output data; and

a judging step of judging quality of said semiconductor device based on said phase difference.

29. A method for testing a semiconductor device as claim in claim 28, further comprising a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data.